AUDIO DSP WITH ANALOG INTERFACE

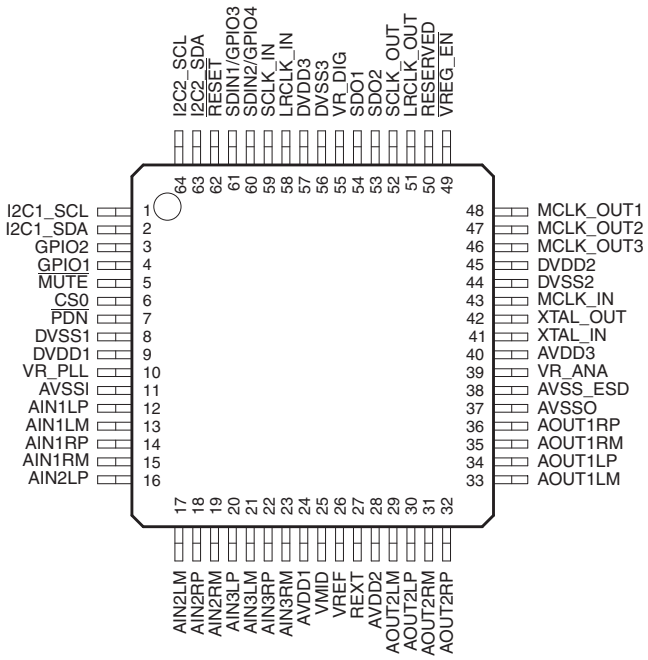
FEATURES

- **High-Quality Audio Performance: 102-dB ADC/105-dB DAC (Typical) DNR**
- **Eight-Channel Programmable Audio DSP (Four-Channel Digital and Four-Channel Analog)**
- **Three Differential Stereo Analog Inputs Multiplexed to Two Stereo Input ADCs**
- **Two Differential Stereo Output DACs**
- **Two Serial Audio Inputs (Four Channels) and Two Serial Audio Outputs (Four Channels)**
- **135-MHz Maximum Speed, >2800 Processing Cycles Per Sample at 48 kHz**
- **512 × Fs XTAL Input in Master Mode, 512 × Fs MCLK_IN in Slave Mode**
- **48-kHz Sample Rate in Master Mode**
- **44.1 or 48-kHz Sample Rate in Slave Mode**
- **48-Bit Data Path and 28-Bit Coefficients**
- **768 Words of 48-Bit Data Memory**
- **1022 Words of 28-Bit Coefficient Memory**
- **3K Words of 55-Bit Program RAM**
- **Hardware Single-Cycle Multiplier (28×48)**
- **2812 Instructions Per Fs**
- **5.88K Words of 24-Bit Delay Memory (122.5 ms at 48 kHz)**
- **Data Formats: Left Justified, Right Justified, and I²S**
- **Two I²C Ports for Slave or Master Download**
- **Single 3.3-V Power Supply**
- **Graphical Development Environment for Audio Processing; e.g., EQ, Algorithm Development**

APPLICATIONS

- **MP3 Docking Systems**
- **Digital Televisions**
- **Mini-Component Audio**

PAG PACKAGE
(TOP VIEW)

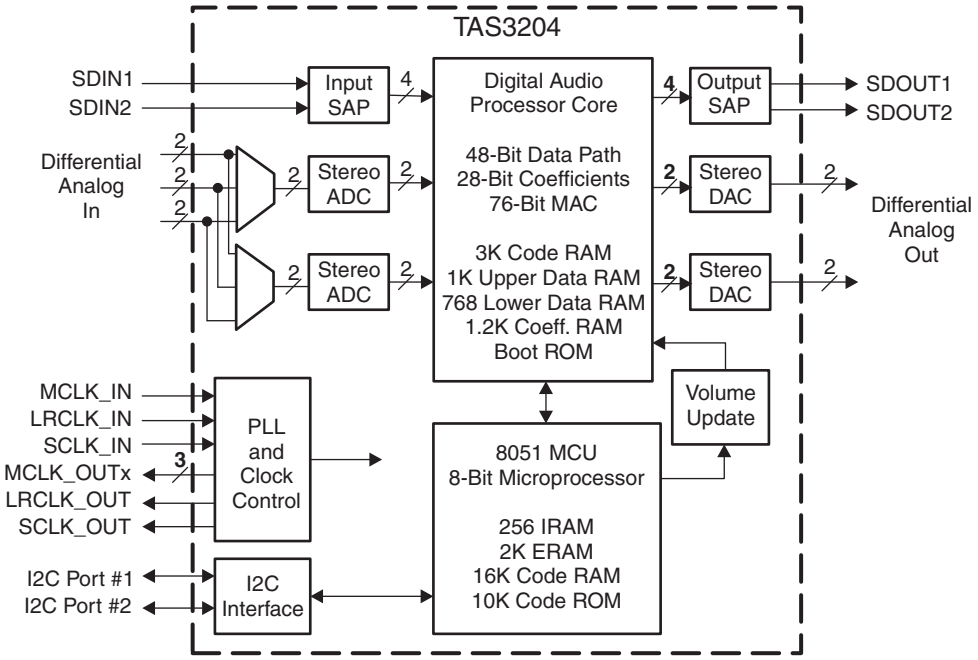


DESCRIPTION/ORDERING INFORMATION

The TAS3204 is an audio system-on-a-chip (SOC) designed for mini/micro systems, multimedia-speaker, and MP3 player docking systems. It includes analog interface functions: three multiplex (MUX) stereo inputs with two stereo analog-to-digital converters (ADCs), two stereo digital-to-analog converters (DACs) with analog outputs consisting of differential stereo line drivers. Four channels of serial digital audio processing are also provided. The TAS3204 has a programmable audio digital signal processor (DSP) that preserves high-quality audio by using a 48-bit data path, 28-bit filter coefficients, and a single cycle 28 × 48-bit multiplier. The programmability feature allows users to customize features in the DSP RAM.

ORDERING INFORMATION

T_A	PLASTIC 64-PIN PQFP (PN)
0°C to 70°C	TAS3204PAG



The TAS3204 is composed of eight functional blocks:

1. Analog input/mux/stereo ADC
2. Two stereo DACs
3. Analog reference system
4. Power supply
5. Clocks, digital PLL, and serial data interface
6. I^2C control interface
7. 8051 microcontroller
8. Audio DSP – digital audio processing

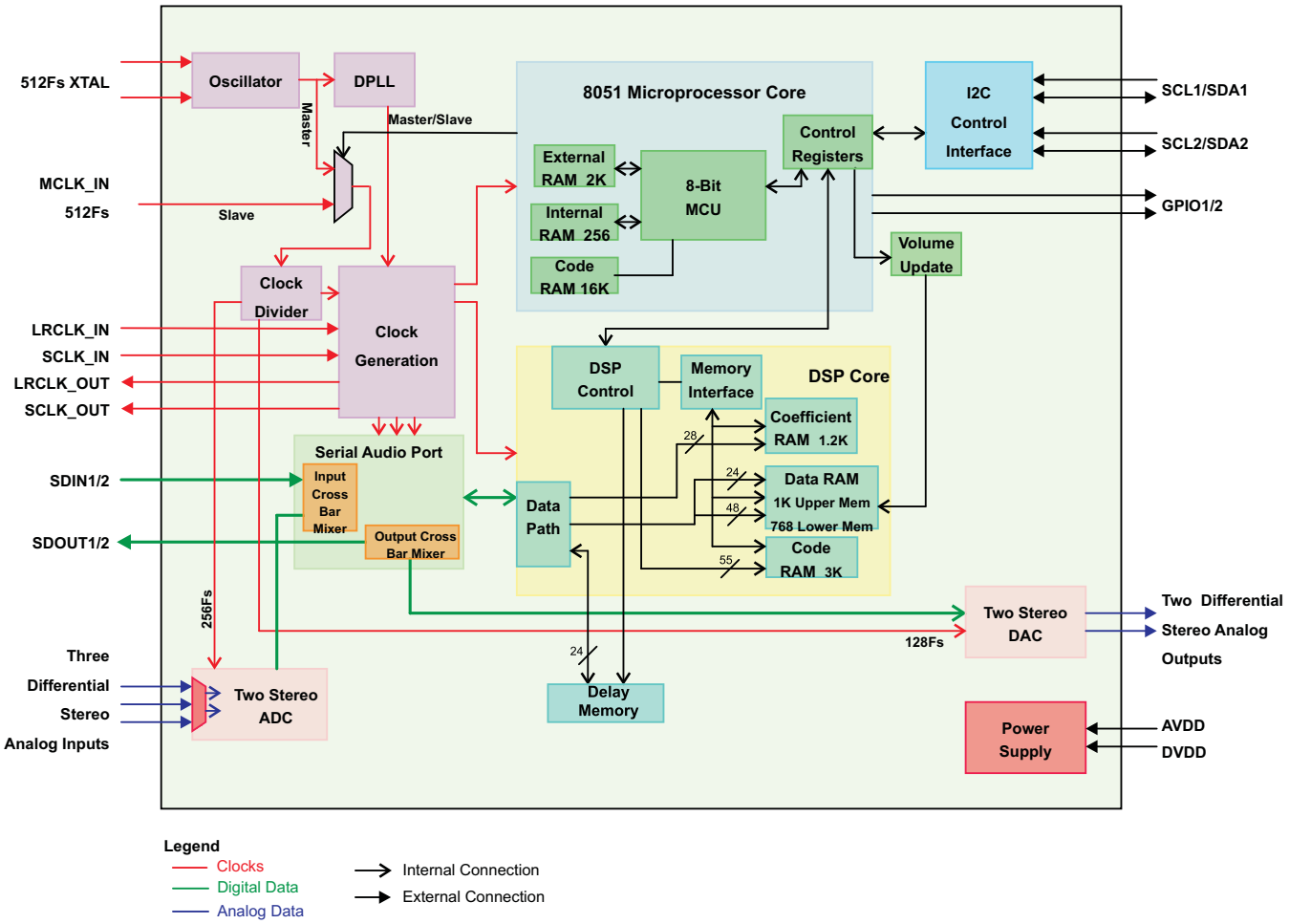


Figure 1. Expanded Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS(1)

over operating temperature range (unless otherwise noted)

DVDD	Digital supply voltage range		–0.5 V to 3.8 V
AVDD	Analog supply voltage range		–0.5 V to 3.8 V
V_I	Input voltage range	3.3-V TTL	–0.5 V to DVDD + 0.5 V
		1.8-V LVCMOS (XTLI)	–0.5 V to 2.3 V
V_O	Output voltage range	3.3-V TTL	–0.5 V to DVDD + 0.5 V
		1.8-V LVCMOS (XTLO)	–0.5 V to 2.3 V(2)
I_{IK}	Input clamp current (V_I < 0 or V_I > DVDD)		±20 µA
I_{OK}	Output clamp current (V_O < 0 or V_O > DVDD)		±20 µA
T_A	Operating free-air temperature range		0°C to 70°C
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Pin XTAL_OUT is the only TAS3204 output that is derived from the internal 1.8-V logic supply. The absolute maximum rating listed is for reference; only a crystal should be connected to XTAL_OUT.

Note:

a. VR_ANA is derived from TAS3204 internal 1.8-V voltage regulator. This terminal must not be used to power external devices.

b. VR_DIG is derived from TAS3204 internal 1.8-V voltage regulator. This terminal must not be used to power external devices.

c. VR_PLL is derived from TAS3204 internal 1.8-V voltage regulator. This terminal must not be used to power external devices.

PACKAGE DISSIPATION RATINGS

Package Description			$T_A \le 25°C$ Power Rating (mW)	Derating Factor Above $T_A = 25°C$ (mW/°C)	$T_A = 70°C$ Power Rating (mW)
Package Type	Pin Count	Package Designator			
TQFP	64	PAG	1869	23.36	818

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
DVDD	Digital supply voltage		3	3.3	3.6	V
AVDD	Analog supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage	3.3-V TTL	2			V
		1.8-V LVCMOS (XTL_IN)	1.2			
V_{IL}	Low-level input voltage	3.3-V TTL			0.8	V
		1.8-V LVCMOS (XTL_IN)			0.5	
T_A	Operating ambient air temperature		0	25	70	°C
T_J	Operating junction temperature		0		105	°C
	Analog differential input			2		V_{RMS}
	Analog output load	Resistance		10		kΩ
		Capacitance		100		pF

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	3.3-V TTL	I_{OH} = –4 mA	2.4			V
		1.8-V LVCMOS (XTL_OUT)	I_{OH} = –0.55 mA	1.44			
V_{OL}	Low-level output voltage	3.3-V TTL	I_{OL} = 4 mA			0.5	V
		1.8-V LVCMOS (XTL_OUT)	I_{OL} = 0.75 mA			0.4	
I_{OZ}	High-impedance output current	3.3-V TTL	$V_I = V_{IL}$			±20	µA

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Low-level input current	3.3-V TTL	$V_I = V_{IL}$			±20	µA
		1.8-V LVCMOS (XTL_IN)	$V_I = V_{IL}$			±20	
I_{IH}	High-level input current	3.3-V TTL	$V_I = V_{IH}$			±20	µA
		1.8-V LVCMOS (XTL_IN)	$V_I = V_{IH}$			±20	
I_{DVDD}	Digital supply current	Normal operation	MCLK_IN = 24.576 MHz, LRCLK = 48 kHz		130		mA
I_{AVDD}	Analog supply current	Normal operation	MCLK_IN = 24.576 MHz, LRCLK = 48 kHz		60		mA
Power Dissipation (Total)	Digital and analog supply current	Normal operation	MCLK_IN = 24.576 MHz, LRCLK = 48 kHz		627		mW
		Standby mode	With voltage regulators on		23		mW
			With voltage regulators off		825		µW
		Reset mode			20		mW
VR_ANA	Internal voltage regulator – analog			1.6	1.8	1.98	V
VR_PLL	Internal voltage regulator – PLL			1.6	1.8	1.98	V
VR_DIG	Internal voltage regulator – digital			1.6	1.8	1.98	V

AUDIO SPECIFICATIONS

T_A = 25°C, AVDD = 3.3 V, DVDD = 3.3 V, Fs = 48 kHz, 1-kHz sine wave full scale, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall performance: input ADC – DAP – DAC – line out	Dynamic range	Evaluation module. A-weighted, –60 dB with respect to full scale		100		dB
	THD+N	Evaluation module. –3 dB with respect to full scale		101		dB
ADC section	Dynamic range	A-weighted, –60 dB with respect to full scale		102		dB
	THD+N	–4 dB with respect to full scale.		93		dB
	Crosstalk	One channel = –3 dB; Other channel = 0 V		84		dB
	Power supply rejection ratio	1 kHz, 100 mVpp on AVDD		57		dB
	Input resistance			20		kΩ
	Input capacitance			10		pF
ADC decimation filter	Pass band edge			0.45 Fs		Hz
	Pass band ripple			±0.01		dB
	Stop band edge			0.55 Fs		Hz
	Stop band attenuation			100		dB
	Group delay			37 ÷ Fs		Sec

AUDIO SPECIFICATIONS (continued)

T_A = 25°C, AVDD = 3.3 V, DVDD = 3.3 V, Fs = 48 kHz, 1-kHz sine wave full scale, over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC section	Differential full scale output voltage				2		V_{RMS}
	Dynamic range		A-weighted, –60 dB with respect to full scale		105		dB
	THD+N		0-dBFS input, 0-dB gain		95		dB
	Crosstalk	DAC to ADC	One channel –3 dBFS; Other channel 0 V		84		dB
		ADC to DAC	One channel –3 dB; Other channel 0 V		84		dB
		DAC to DAC	One channel –3 dBFS; Other channel 0 V		84		dB
	Power supply rejection ratio		1 kHz, 100 mVpp on AVDD		56		dB
	DC offset		With respect to V_{REF}				mV
DAC interpolation filter	Pass band edge				0.45 Fs		Hz
	Pass band ripple				±0.06		dB
	Transition band				1.45 Fs to 0.55 Fs		Hz
	Stop band edge				7.4 Fs		Hz
	Stop band attenuation				–65		dB
	Filter group delay				21 ÷ Fs		Sec

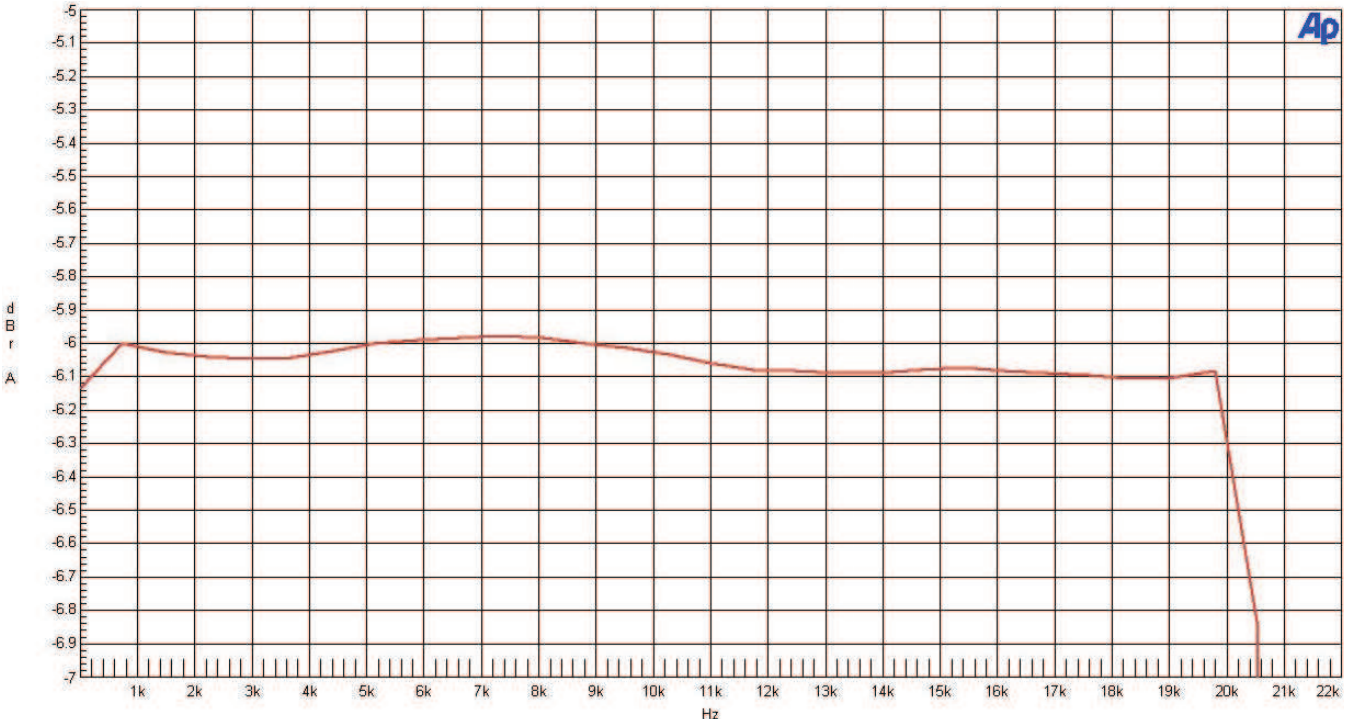


Figure 2. Frequency Response (ADC-DAC)

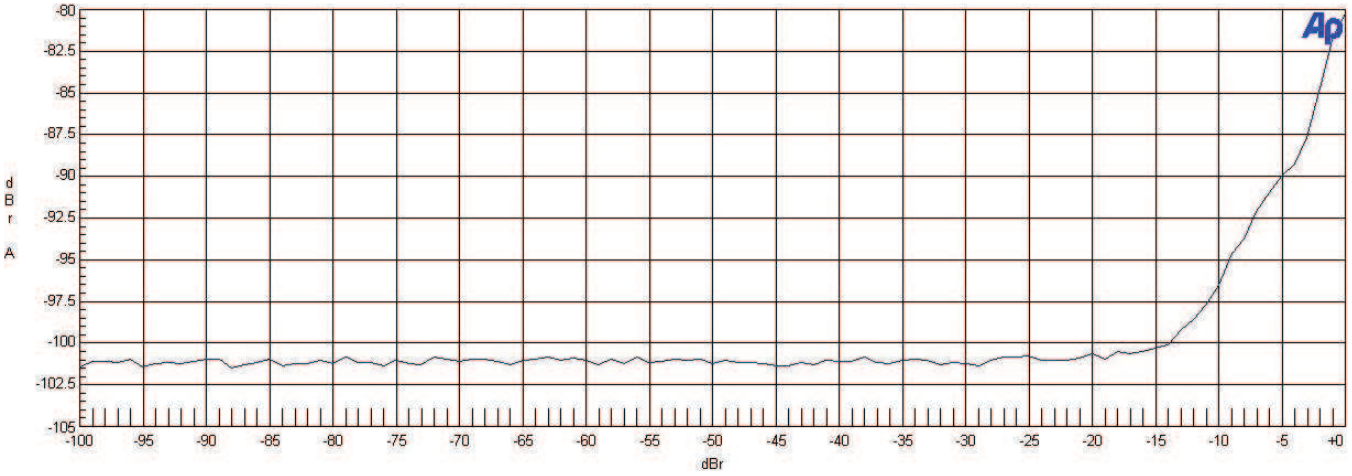


Figure 3. THD + N (ADC-DAC)

TIMING CHARACTERISTICS

Master Clock

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(XTAL\_IN)}$	Frequency, XTAL_IN (1/ $t_{c(1)}$)		See (1)		512Fs		Hz
$t_{c(1)}$	Cycle time, XTAL_IN				1÷512Fs		Sec
$f_{(MCLK\_IN)}$	Frequency, MCLK_IN (1/ $t_{c(2)}$)				512Fs		Hz
$t_{w(MCLK\_IN)}$	Pulse duration, MCLK_IN high		See (2)	0.4 $t_{c(2)}$	0.5 $t_{c(2)}$	0.6 $t_{c(2)}$	ns
	Crystal frequency deviation					50	ppm
$f_{(MCLKO)}$	Frequency, MCLKO (1/ $t_{c(3)}$)				256Fs		Hz
$t_{r(MCLKO)}$	Rise time, MCLKO		C_L = 30 pF			15	ns
$t_{f(MCLKO)}$	Fall time, MCLKO		C_L = 30 pF			15	ns
$t_{w(MCLK\_IN)}$	Pulse duration, MCLKO high		See (3)		H_{MCLKO}		ns
	MCLKO jitter	XTAL_IN master clock source			80		ps
		MCLK_IN master clock source	See (4)				ps
$t_{d(MI-MO)}$	Delay time, MCLK_IN rising edge to MCLKO rising edge	MCLKO = MCLK_IN	See (5)			20	ns
		MCLKO < MCLK_IN	See (5) (6)			20	ns

(1) Duty cycle is 50/50.
(2) Period of MCLK_IN = T_{MCLK_IN} = $1/f_{MCLK\_IN}$
(3) H_{MCLKO} = 1/(2 × MCLKO). MCLKO has the same duty cycle as MCLK_IN when MCLKO = MCLK_IN. When MCLKO = 0.5 MCLK_IN or 0.25 MCLK_IN, the duty cycle of MCLKO is typically 50%.
(4) When MCLKO is derived from MCLK_IN, MCLKO jitter = MCLK_IN jitter
(5) Only applies when MCLK_IN is selected as master source clock
(6) Also applies to MCLKO falling edge when MCLKO = MCLK_IN/2 or MCLK_IN/4

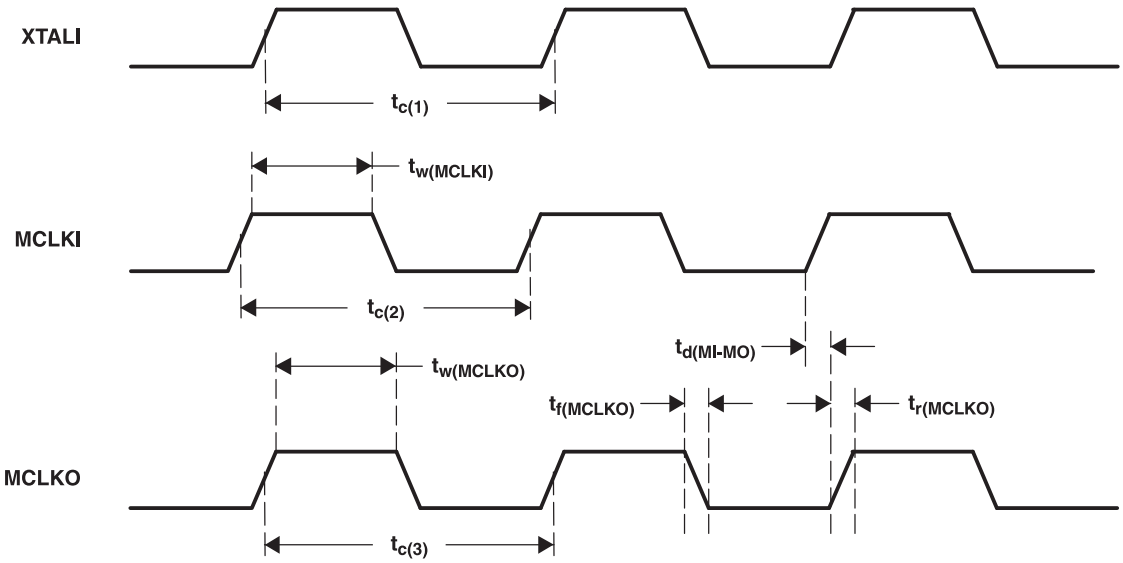


Figure 4. Master Clock Signal Timing Waveforms

Serial Audio Port, Slave Mode

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LRCLK}	Frequency, LRCLK (f_S)				48	kHz
$t_{w(SCLKIN)}$	Pulse duration, SCLKIN high	See (1)	0.4 $t_{c(SCLKIN)}$	0.5 $t_{c(SCLKIN)}$	0.6 $t_{c(SCLKIN)}$	ns
f_{SCLKIN}	Frequency, SCLKIN	See (2)		64 F_S		MHz
t_{pd1}	Propagation delay, SCLKIN falling edge to SDOUT				16	ns
t_{su1}	Setup time, LRCLK to SCLKIN rising edge		10			ns
t_{h1}	Hold time, LRCLK from SCLKIN rising edge		5			ns
t_{su2}	Setup time, SDIN to SCLKIN rising edge		10			ns
t_{h2}	Hold time, SDIN from SCLKIN rising edge		5			ns
t_{pd2}	Propagation delay, SCLKIN falling edge to SCLKOUT2 falling edge				15	ns

(1) Period of SCLKIN = $T_{SCLKIN} = 1/f_{SCLKIN}$
(2) Duty cycle is 50/50.

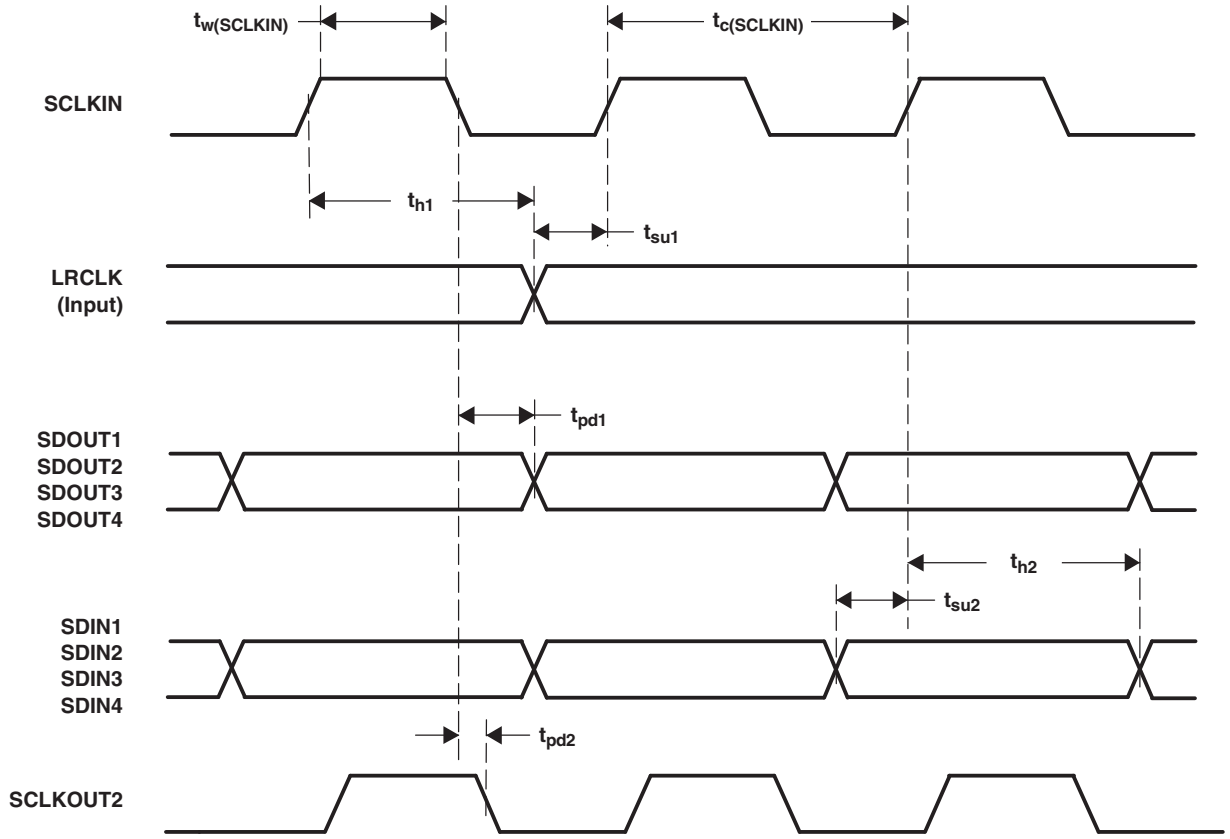


Figure 5. Serial Audio Port Slave Mode Timing Waveforms

Serial Audio Port Master Mode Signals (TAS3204)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(LRCLK)}$	Frequency LRCLK	C_L = 30 pF		48		kHz
$t_{r(LRCLK)}$	Rise time, LRCLK (1)	C_L = 30 pF			12	ns
$t_{f(LRCLK)}$	Fall time, LRCLK (1)	Duty cycle is 50/50			12	ns
$f_{(SCLKOUT)}$	Frequency, SCLKOUT	C_L = 30 pF		$64F_S$		MHz
$t_{r(SCLKOUT)}$	Rise time, SCLKOUT	C_L = 30 pF			12	ns
$t_{f(SCLKOUT)}$	Fall time, SCLKOUT	C_L = 30 pF			12	ns
$t_{pd1(SCLKOUT)}$	Propagation delay, SCLKOUT falling edge to LRCLK edge				5	ns
t_{pd2}	Propagation delay, SCLKOUT falling edge to SDOUT1-2				5	ns
t_{su}	Setup time, SDIN to SCLKOUT rising edge		25			ns
t_h	Hold time, SDIN from SCLKOUT rising edge		30			ns

(1) Rise time and fall time measured from 20% to 80% of maximum height of waveform.

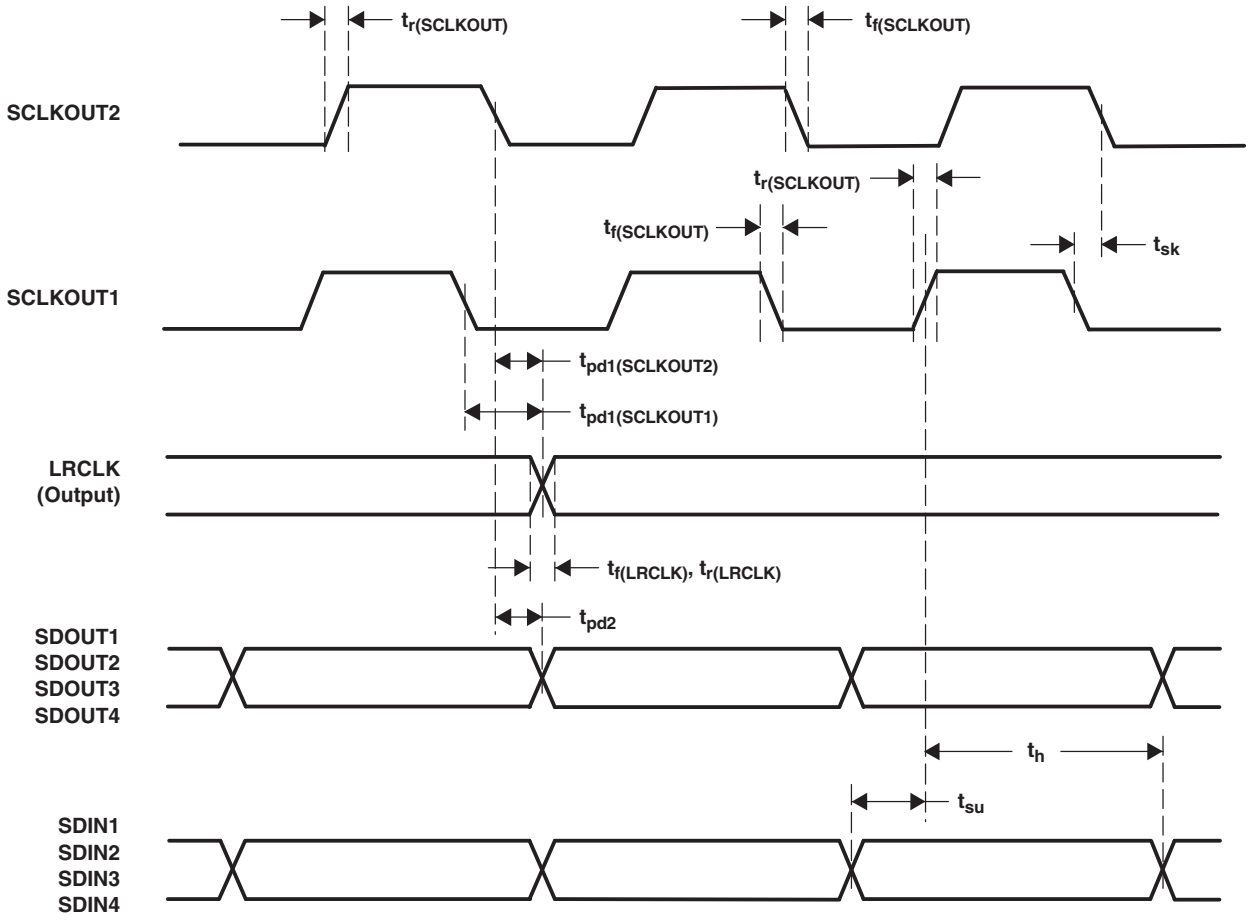


Figure 6. Serial Audio Port Master Mode Timing Waveforms

Pin-Related Characteristics of the SDA and SCL I/O Stages for F/S-Mode I²C-Bus Devices

PARAMETER		TEST CONDITIONS	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
V_{IL}	LOW-level input voltage		–0.5	0.8	–0.5	0.8	V
V_{IH}	HIGH-level input voltage		2		2		V
V_{hys}	Hysteresis of inputs		N/A	N/A	0.05 V_{DD}		V
V_{OL1}	LOW-level output voltage (open drain or open collector)	3-mA sink current			0	0.4	V
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	Bus capacitance from 10 pF to 400 pF		250	7 + 0.1 C_b (1)	250	ns
I_I	Input current, each I/O pin		–10	10	–10 (2)	10 (2)	µA
$t_{SP(SCL)}$	SCL pulse duration of spikes that must be suppressed by the input filter		N/A	N/A	14 (3)		ns
$t_{SP(SDA)}$	SDA pulse duration of spikes that must be suppressed by the input filter		N/A	N/A	22 (3)		ns
C_I	Capacitance, each I/O pin			10		10	pF

(1) C_b = capacitance of one bus line in pF. The output fall time is faster than the standard I²C specification.
(2) The I/O pins of fast-mode devices must not obstruct the SDA and SDL lines if V_{DD} is switched off.
(3) These values are valid at the 135-MHz DSP clock rate. If DSP clock is reduced by half, the t_{SP} doubles.

Bus-Related Characteristics of the SDA and SCL I/O Stages for F/S-Mode I²C-Bus Devices

all values are referred to V_{IHmin} and V_{ILmax} (see SubSec1 5.4)

PARAMETER		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency	0	100	0	400 (1)	kHz
t_{HD-STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4		0.6		µs
t_{LOW}	LOW period of the SCL clock	4.7		1.3		µs
t_{HIGH}	HIGH period of the SCL clock	4		0.6		µs
t_{SU-STA}	Setup time for repeated START	4.7		0.6		µs
t_{SU-DAT}	Data setup time	250		100		µs
t_{HD-DAT}	Data hold time (2)(3)	0	3.45	0	0.9	µs
t_r	Rise time of both SDA and SCL signals		1000	20 + 0.1 C_b (4)	300	ns
t_f	Fall time of both SDA and SCL		300	20 + 0.1 C_b (4)	300	ns
t_{SU-STO}	Setup time for STOP condition	4		0.6		µs
t_{BUF}	Bus free time between a STOP and START condition	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF
V_{nL}	Noise margin at the LOW level for each connected device (including hysteresis)	0.1V_{DVDD}		0.1V_{DVDD}		V
V_{nH}	Noise margin at the HIGH level for each connected device (including hysteresis)	0.2V_{DVDD}		0.2V_{DVDD}		V

(1) In master mode, the maximum speed is 375 kHz.
(2) Note that SDA does not have the standard I²C specification 300-ns internal hold time. SDA must be valid by the rising and falling edges of SCL. TI recommends that a 2-kΩ pullup resistor be used to avoid potential timing issues.
(3) A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU-DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r-max} + t_{SU-DAT} = 1000 + 250 = 1250$ ns (according to the standard-mode I²C bus specification) before the SCL line is released.
(4) C_b = total capacitance of one bus line in pF

NOTE:

SDA does not have the standard I²C specification 300-ns internal hold time. SDA must be valid by the rising and falling edges of SCL.

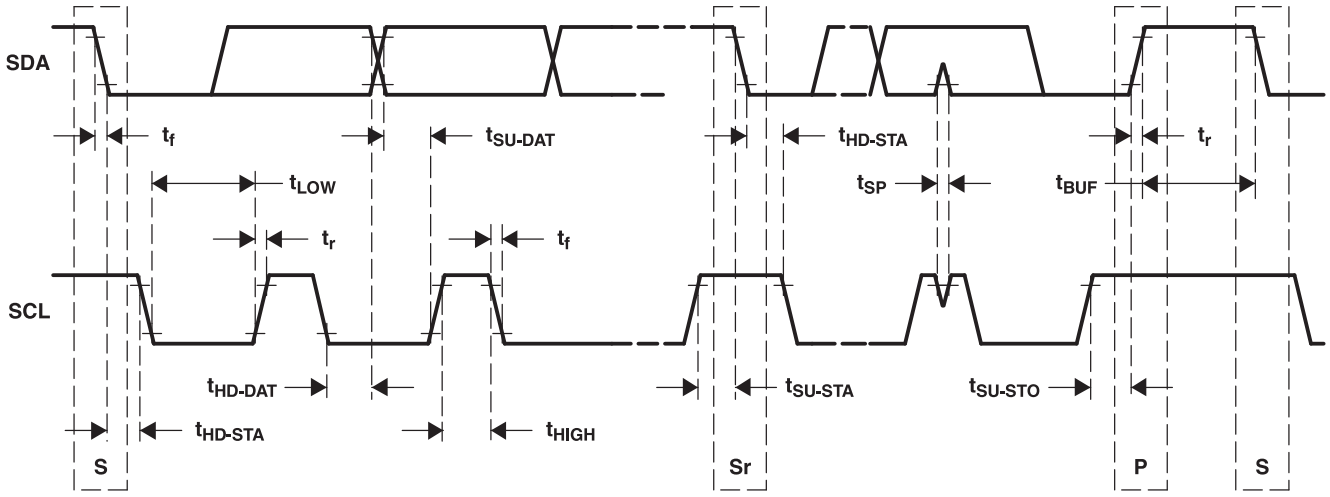


Figure 7. Start and Stop Conditions Timing Waveforms

Recommended I²C Pullup Resistors

It is recommended that the I²C pullup resistors R_P be 4.7 kΩ (see Figure 8). If a series resistor is in the circuit (see Figure 9), then the series resistor R_S should be less than or equal to 300 Ω.

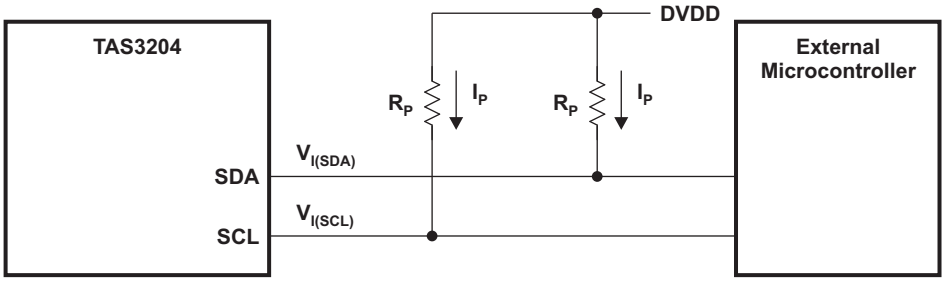
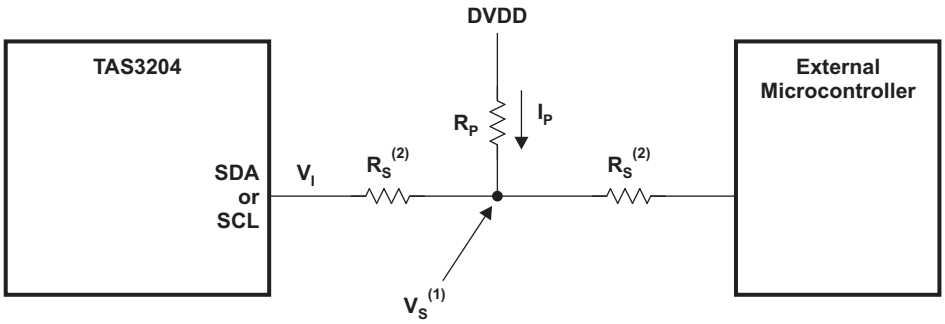


Figure 8. I²C Pullup Circuit (With No Series Resistor)



(1) $V_S = DVDD \times R_S/(R_S - R_P)$. When driven low, $V_S << V_{IL}$ requirements.

(2) $R_S \leq 300\ \Omega$

Figure 9. I²C Pullup Circuit (With Series Resistor)

Reset Timing

control signal parameters over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(RESET)}$	Pulse duration, RESET active	200		ns
$t_{r(DMSTATE)}$	Time to outputs inactive		100	µs
$t_{r(run)}$	Time to enable I^2C	50		ms

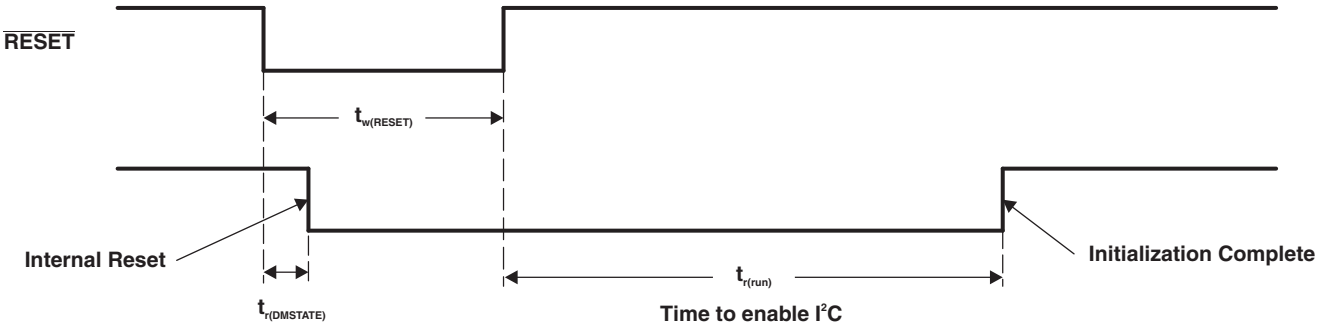


Figure 10. Reset Timing

APPLICATION INFORMATION

Schematics

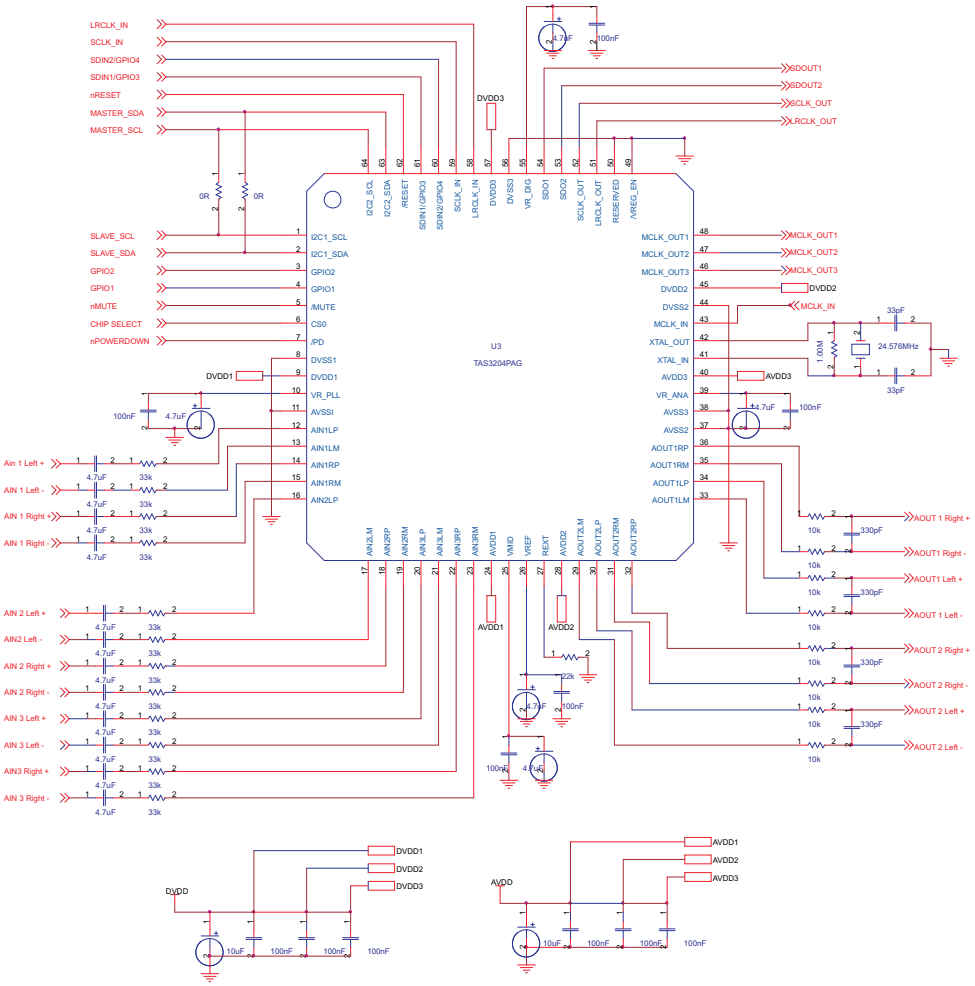
Figure 11 shows a typical TAS3204 application. In this application the following conditions apply:

- TAS3204 is in clock-master mode. The TAS3204 generates MCLK_OUT1, SCLK_OUT, and LRCLOK_OUT.
- XTAL_IN = 24.576 MHz
- I^2C register 0x00 contains the default settings, which means:
  - Audio data word size is 24-bit input and 24-bit output.
  - Serial data format is 2-channel, I^2S for input and output.
  - I^2C data transfer is approximately 400 kbps for both master and slave I^2C interfaces.
  - Sample frequency (f_S) is 48 kHz, which means that f_{LRCLK} = 48 kHz and f_{SCLKIN} = 3.072 MHz.
- Application code and data are loaded from an external EEPROM using the master I^2C interface.
- Application commands come from the system microprocessor to the TAS3204 using the slave I^2C interface.

Good design practice requires isolation between the digital and analog power as shown. Power supply capacitors of 10 μF and 0.1 μF should be placed near the power supply pins AVDD (AVSS) and DVDD (DVSS).

The TAS3204 reset needs external glitch protection. Also, reset going HIGH should be delayed until TAS3204 internal power is good (~200 μs after power up). This is provided by the 1-kΩ resistor, 1-μF capacitor, and diode placed near the RESET pin.

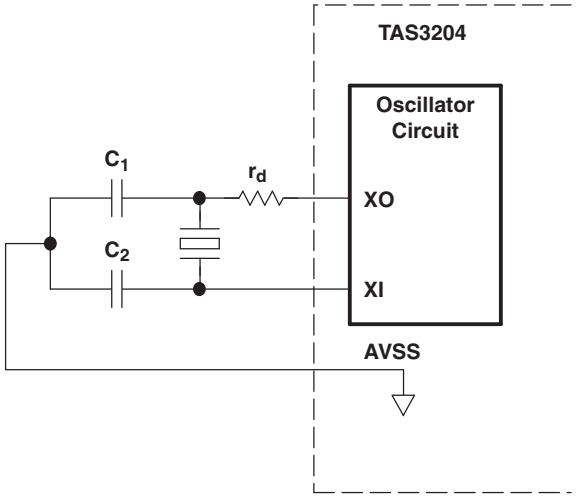
It is recommended that a 4.7-μF capacitor (fast ceramic type) be placed near pin 28 (VR_DIG). This pin must not be used to source external components.



A. Capacitors should be placed as close as possible to the power supply pins.

Figure 11. Typical Application Diagram

Recommended Oscillator Circuit



- Crystal type = parallel-mode, fundamental-mode crystal
- r_d = drive-level control resistor – vendor specified
- C_L = Crystal load capacitance (capacitance of circuitry between the two terminals of the crystal)
- $C_L = (C_1 \times C_2)/(C_1 + C_2) + C_S$ (where C_S = board stray capacitance, ~2 pF)

PACKAGING INFORMATION

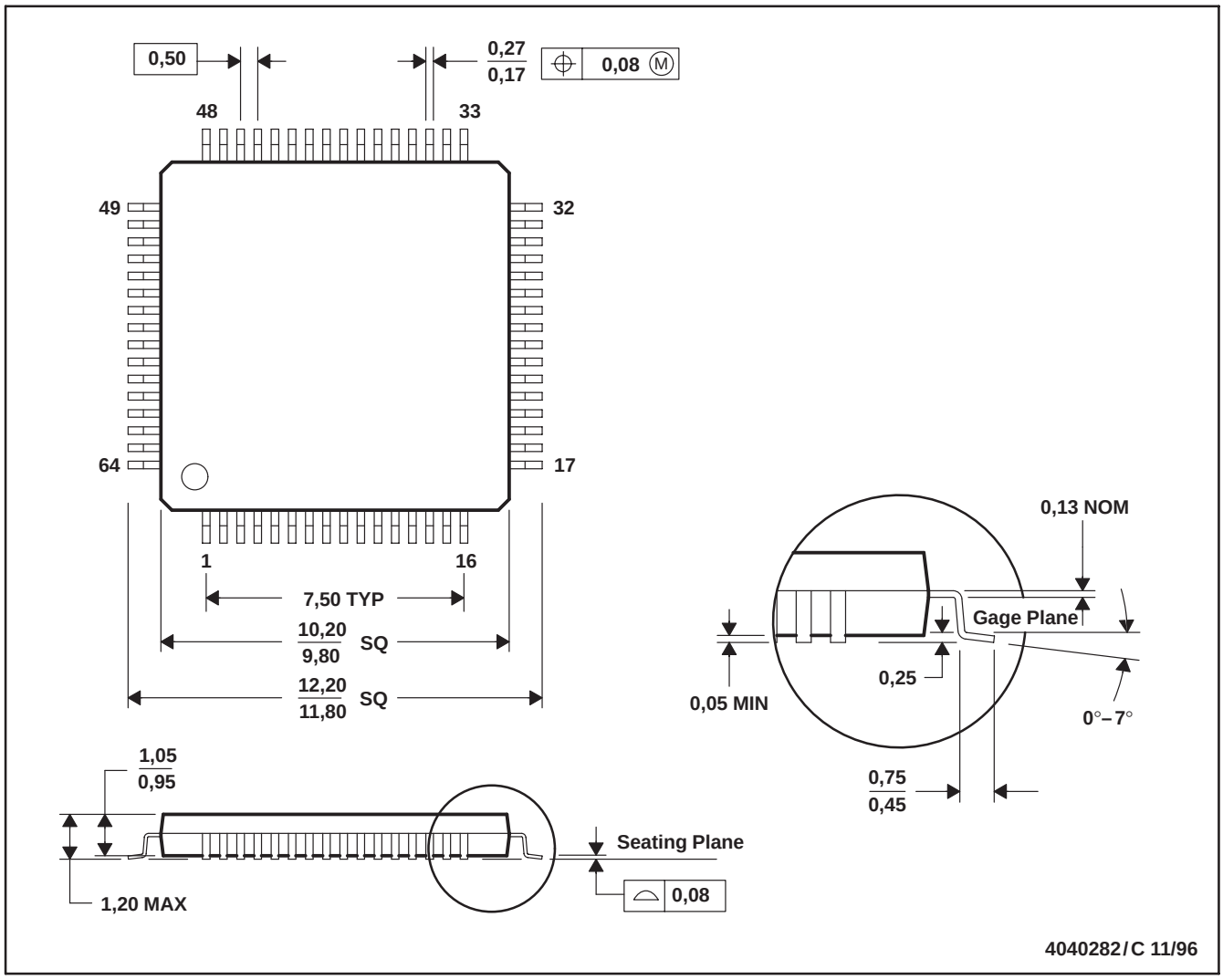
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TAS3204PAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
TAS3204PAGR	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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